Nikolaos Makris

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Profile Summary

I am a Semiconductor Research Engineer with more than 10 years of experience in R&D projects related with static and dynamic measurements, characterization and device modeling of various commercial and research oriented CMOS and wide bandgap processes. Deep understanding of semiconductor devices' operation and performance issues.

- ➔ Extensive hands-on experience setting-up and performing on-wafer DC,CV and RF measurements.
- ➔ Design oriented characterization and modeling of CMOS technology node's statistical behavior.
- ➔ Utilizing high level languages for modeling and characterization purposes (ex. Java application for modeling and characterization (MOSGUI project), measurement and data acquisition lab setups using PyVISA).
- ➔ Extensive experience in commercial and open-source simulators (ex. NGSPICE, Cadence Spectre) and EDA tools (ex. KeySight ICCAP).
- ➔ Verilog-A Charge based Compact Model development (EKV3, CJM), customization and integration in analog simulators.
- ➔ Authored or co-authored 11 journal and 26 conference papers.

Starting 2016, I am with Microelectronics Research Group (MRG) / Institute of Electronic Structure and Laser(IESL) / Foundation for Research and Technology-Hellas (FORTH) working on development, modeling and characterization of SiC JFETs and GaN HEMTs.

Awards/Acknowledgments:

- Received "**Best Paper Award** in **48th European Solid-State Device Research Conference (ESSDERC 2018),** Sept. 3-6, 2018 Dresden (Germany)"
- Received "**Best Paper Award** in **41st IEEE International Semiconductor Conference (CAS 2018)**, Oct. 10-12, 2018 Sinaia (Romania)"

Education

PhD
Dec. 2015 – Present
School of Electronic and Computer Engineering, Technical University of Crete (TUC), Chania, Greece
Title: "Charge based FET Modelling"
Supervisor: Assis. Prof. M. Bucher
➔ DG JFET & MESFET characterization and charge based modelling

MSc
Dec. 2006 - Jul. 2011
School of Electronic and Computer Engineering, Technical University of Crete (TUC), Chania, Greece
Thesis Title: "Characterization and RF Design Aspects in Advanced CMOS Technology."
Supervisor : Assis. Prof. M. Bucher
➔ MOSFET DC Measurements and Characterization with temperature scaling (Summit 10600 probe station,

HP4142A and Temptronic TP030000 temperature controller) covering aspects like intrinsic gain and DIBL temperature behaviour.

Bachelor of Electronics and Computer Engineering
Oct. 2000 - Oct. 2006
School of Electronic and Computer Engineering, Technical University of Crete (TUC), Chania, Greece
Thesis Title: "Design and Modeling of integrated inductors in RF applications."
Supervisor : Dr. Apostolos Samelis
➔ Development of octagonal integrated inductors' design kit in Agilent's ADS environment covering aspects like automatic layout design, design rule check, and inductor modelling.

Training

IDESA Training Course
1-5 Dec. 2008
Interuniversitair Micro-Electronica Centrum (IMEC), Leuven, Belgium
Advanced RF Implementation Flow
➔ Modelling issues, microwave passive component design and simulation, testing and microwave measurements, mismatch modelling and simulation, mixed-modes SoC design and simulation, analog and RF cell trimming using digital functions, design verification, circuit packaging and ESD-protection.

Work/Research Experience

2011 – Present **R&D Project – EKV3 Charge based model**
Position: Member of EKV3 development team
➔ Verilog-A code developing, maintenance and testing of EKV3 charge based Compact Model.
➔ Handling bugs and issues indicated from academia and industrial users.
Electronics Laboratory Technical University of Crete (T.U.C.), supervisor: Assis. Prof. M. Bucher

Dec. 2016 – Present **R&D Projects for IESL / FORTH**
Position: Research Engineer
➔ DC, CV and RF characterization and modeling of SiC Power JFETs and GaN HEMTs.
➔ TCAD SiC JFET / GaN HEMT simulations for verification and improvement of the current SiC/GaN processes.
Microelectronics Research Group (MRG) / Institute of Electronic Structure and Laser(IESL) / Foundation for Research and Technology-Hellas (FORTH), supervisors: Principal Researcher Dr. K. Zekentes / Principal Researcher Dr. G. Konstantinidis

May 2020 –Oct. 2020 **R&D Project for external industrial partner**
Position: Software Developer

- ➔ Upgrade to v. 2.0.5 and addition of extra capabilities to Java based graphical tool (MOSGUI) for MOS transistors. Some of MOSGUI's upgrades were:
  - ✓ Extension of import capabilities (more than 2000 data files were imported).
  - ✓ Improvements in data and simulation visualizations.
  - ✓ Automated scaling plots threshold voltage, on/off current and mobility versus device length / width.

Jan. 2020 – Apr. 2020 **R&D Project for external industrial partner**

Position: Research Engineer

- ➔ Low frequency noise measurements and characterization of LV MOSTs in 110nm CMOS process

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Dec. 2018 – Dec. 2019 **R&D Project for Conseil Européen pour la Recherche Nucléaire (CERN)- (CERN2º)**

Position: Research Engineer

- ➔ Research of MOSFET performance degradation due to high TID radiation effects.
- ➔ 65nm design kit extension to cover the radiation effects (up to 500MRad) in LVT and HVT standard and enclosed gate layout MOSFETs from 25 up to -30ºC. Candidate technology for High-Luminosity Large Hadron Collider (HL-LHC).

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Jun. 2018 – Nov. 2018 **R&D Project for external industrial partner**

Position: Research Engineer

- ➔ HV-LD-MOSFET analysis, parameter extraction and modeling using customized HISIM 2.10 model.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Dec. 2017 – May. 2018 **R&D Project for Conseil Européen pour la Recherche Nucléaire (CERN)- (CERN1º)**

Position: Research Engineer

- ➔ Research of MOSFET performance degradation due to high TID radiation effects.
- ➔ 65nm design kit extension to cover the radiation effects (up to 500MRad) in SVT standard and enclosed gate layout MOSFETs from 25 up to -30ºC. Candidate technology for High-Luminosity Large Hadron Collider (HL-LHC).

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Jan. 2016 – Mar. 2016 **R&D Project for external industrial partner**

Position: Research Engineer

- ➔ Designating and characterizing MOSFET sub-threshold variability issues using custom JAVA based application.
- ➔ Developing, testing(Monte Carlo simulations) and issuing EKV3 custom version incorporating the characterization equations.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Jan. 2015 – Jun.2016 **R&D Project for external industrial partner**

Position: Research Engineer

- ➔ Characterization and modelling of 110nm CMOS technology.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Jul. 2014 – Dec. 2014 **R&D Project for external industrial partner**

Position: Software Developer

- ➔ Development of Java based graphical tool (MOSGUI) for MOS transistor data for modelling and characterization purposes. MOSGUI's capabilities are:
  - ✓ Importing, categorizing and visualizing of MOSFET transfer and output characteristics and producing trans-conductance graphs.
  - ✓ Automating Spectre simulation and plotting the results versus data.
  - ✓ Exporting pdf reports.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Jan. 2014 – Jun. 2014 **R&D Project for external industrial partner**

Position: Research Engineer

- ➔ EKV3.0 – EKV 2.6 MOST modelling in 0.18um CMOS process.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Apr. 2013 – Dec. 2013 **R&D Project "NexGenMilliWave: Next Generation Millimeter Wave Backhaul Radio."**

Position: Research Engineer

- ➔ Research in characterization and modelling of RF CMOS devices.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Aug. 2012 – Nov. 2013 **R&D Project "ANTI-SiC: Development of new transistors and inverter for photovoltaic systems based on Silicon Carbide."**

Position: Research Engineer

- ➔ Development of Verilog-A charge based JFET model covering DC and AC operation.
- ➔ DC and small signal characterization of on wafer and packaged JFETs.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Sept. 2012 – Nov. 2012 **Internship in ADMOS GmbH , Frickenhausen , Germany (COmpact MOdelling Network (COMON)– FP7-PEOPLE-2007)**

Position: Research Engineer

- ➔ Comparison between different self heating characterization methods.
- ➔ Developing measurement methods to determine self heating effects in high Voltage MOS transistors.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Apr. 2012 – Apr. 2012 **R&D Project for external industrial partner**

Position: Research Engineer

- ➔ 0.18 CMOS process LV & MV MOSTs modelling.

Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete

(T.U.C.),supervisor: Assis. Prof. M. Bucher

Jan. 2012 – Mar. 2012 **R&D Project "NANOsympraxis: Multigate MOSFET nanotransistors: compact models for current and noise – development of automated design tools for nanoelectronics."**
Position: Research Engineer
➔ Compact Modelling and parameter extraction of multigate MOSFETs.
Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Oct. 2011 – Dec. 2011 **R&D Project "NANOsympraxis: Multigate MOSFET nanotransistors: compact models for current and noise – development of automated design tools for nanoelectronics."**
Position: Research Engineer
➔ Compact Modelling and parameter extraction of multigate MOSFETs.
Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Mar. 2011 – Apr. 2011 **R&D Project "NexGenMilliWave: Next Generation Millimeter Wave Backhaul Radio."**
Position: Research Engineer
➔ CMOS 90nm RF Model Library evaluation.
Telecommunication Systems Research Institute(T.S.I.), Technical University of Crete (T.U.C.),supervisor: Assis. Prof. M. Bucher

Technical Skills and Competences

- ➔ On Wafer(Cascade Prober) DC (HP4142 , HP4145, Keithley 4200), RF (HP 8510C) and CV (Agilent E4980A) Measurements' setup of MOSFET/HEMT/JFET processes using Agilent's ICCAP, SweepMe! or custom JAVA/Python application (using E5810A GPIB gateway / 82357B USB to GPIB interface) as Measuring and Characterization Software.
  - ✓ DC/CV temperature characterization (up to 393K).
- ➔ Temperature varying DC (using HP4142 with four-terminal (Kelvin) sensing) and CV Measurements (custom Bias Tees) and Characterization of packaged standard HV MOSFETs and JFETs.

Software Skills and Competences

- ➔ Experienced user of Microsoft Windows and several Linux distributions (CentOS, Ubuntu and Suse).
- ➔ Extensive use of Linux terminal and Linux Shell Script Language.
- ➔ Good Knowledge of **Keysight's Application Extension Language (AEL)** and **Keysight's ICCAP macro language**.
- ➔ Limited experience in **Cadence's OCEAN** and **SKILL** code development.
- ➔ Device and circuit simulation using **Cadence's ADE, QUCS** and **LTSPICE**.
- ➔ Mathematical Tools used:
  - ✓ **Matlab**, **Mathcad** and **WolframAlpha**.
- ➔ **Silvaco TCAD** simulations.
- ➔ Good knowledge of **C/C++** language.
- ➔ Good knowledge of **Python**
  - ✓ Extensive usage of **JupyterLab** for modelling, characterization and measurement statistical analysis.

- ➔ **JFETLAB**
  - ✓ A Double Gate (DG) JFET simulation tool published in nanohub.org.
- ➔ Experienced **Verilog-A** developer.
  - ✓ **EKV3 Verilog-A** compact MOSFET model version 302.00 released in 2015 and distributed in Cadence, Synopsys, Keysight and Cigma - Design.
  - ✓ **EKV3 Verilog-A** to C language translation and integration using ADMSXML code generator for Cadence CMI, Quite Universal Circuit Simulator (QUCS) and NGSpice.
  - ✓ **Verilog-A DG JFET** charge based model Development.
- ➔ **JAVA application development** for:
  - ✓ measuring (for instance JAVA application using jGpibEnet library with E5810A GPIB gateway for DC measurements (HP4142B) in Linux environment (Ubuntu)),
  - ✓ characterization and modelling purposes of FET devices (MOSGUI) .
- ➔ Administrative duties (PDK installation, tools installation, licensing setup etc.), from 2006 to 2016, for Cadence and Agilent Products used at Electronics Laboratory of the Department of Electronic and Computer Engineering, Technical University of Crete.

Languages

- ➔ Greek (Mother Tongue)
- ➔ English
  - ✓ Reading / Listening - Proficient User
  - ✓ Writing / Speaking - Independent User

Publications (indicative list)

Journals (total: 11)

1. D.Stefanakis, **N. Makris**, K. Zekentes and D. Tassis **"**Comparison of Impact Ionization Models for 4H-SiC Along the< 0001> Direction, Through Breakdown Voltage Simulations at Room Temperature**",** vol.68, no. 5, pp. 2582-2586, Mar. 2021, doi: 10.1109/TED.2021.3066143
2. **N. Makris**, M. Bucher, L. Chevas, F. Jazaeri and J. -M. Sallese, "Free Carrier Mobility, Series Resistance, and Threshold Voltage Extraction in Junction FETs," in IEEE Transactions on Electron Devices, vol. 67, no. 11, pp. 4658-4661, Nov. 2020, doi: 10.1109/TED.2020.3025841.
3. **N. Makris**, M. Bucher, F. Jazaeri and J. Sallese, "CJM: A Compact Model for Double-Gate Junction FETs," in IEEE Journal of the Electron Devices Society, vol. 7, pp. 1191-1199, 2019, doi: 10.1109/JEDS.2019.2944817
4. **N. Makris**, F. Jazaeri, J. Sallese, R. K. Sharma and M. Bucher, "Charge-Based Modeling of Long-Channel Symmetric Double-Gate Junction FETs--Part I: Drain Current and Transconductances," in IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 2744-2750, July 2018. doi: 10.1109/TED.2018.2838101
5. **N. Makris**, F. Jazaeri, J. Sallese and M. Bucher, "Charge-Based Modeling of Long-Channel Symmetric Double-Gate Junction FETs--Part II: Total Charges and Transcapacitances," in IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 2751-2756, July 2018. doi: 10.1109/TED.2018.2838090
6. F. Jazaeri, **N. Makris**, A. Saeidi, M. Bucher and J. Sallese, "Charge-based Model for Junction FETs," in IEEE Transactions on Electron Devices, vol. 65, no. 7, pp. 2694-2698, July 2018. doi: 10.1109/TED.2018.2830972
7. N. Mavredakis, **N. Makris**, P. Habas and M. Bucher, "Charge-Based Compact Model for Bias-Dependent Variability of 1/f Noise in MOSFETs," in IEEE Transactions on Electron Devices, vol. 63, no. 11, pp. 4201-4208, Nov. 2016. doi: 10.1109/TED.2016.2608722
8. Antonopoulos, M. Bucher, K. Papathanasiou, N. Mavredakis, N**. Makris**, R. K. Sharma, P. Sakalas, M. Schroter, "CMOS Small-Signal and Thermal Noise Compact Modeling at High Frequencies", *IEEE Trans. on Electron Devices,* Vol. 60, N° 11, pp. 3726-3733, Nov. 2013. doi ieeexplore

Conferences(total: 26)

1. **N. Makris**, L. Chevas and M. Bucher, "Compact Modeling of Low Frequency Noise and Thermal Noise in Junction Field Effect Transistors," ESSDERC 2019 - 49th European Solid-State Device Research Conference (ESSDERC), Cracow, Poland, 2019, pp. 198-201, doi: 10.1109/ESSDERC.2019.8901775.
2. **N. Makris**, K. Zekentes, M. Bucher, "Compact Modeling of SiC and GaN Junction FETs at High Temperature", European Conference on Silicon Carbide and Related Materials (ECSCRM), Materials Science Forum, vol. 963, Trans Tech Publications, Ltd., July 2019, pp. 683–687. Crossref, doi:10.4028/www.scientific.net/msf.963.683.
3. M. Kayambaki, **N. Makris**, K. Tsagaraki, H. Peyré, A. Stavrinidis, G. Konstantinidis, K. Zekentes, "4H-SiC p-type doping determination from secondary electrons imaging", European Conference on Silicon Carbide and Related Materials (ECSCRM), Materials Science Forum, vol. 963, Trans Tech Publications, Ltd., July 2019, pp. 328–331. Crossref, doi:10.4028/www.scientific.net/msf.963.328.
4. **(Best Paper Award) N. Makris**, M. Bucher, F. Jazaeri and J. Sallese, "A Compact Model for Static and Dynamic Operation of Symmetric Double-Gate Junction FETs," 2018 48th European Solid-State Device Research Conference (ESSDERC), Dresden, 2018, pp. 238-241. doi: 10.1109/ESSDERC.2018.8486848
5. K. Tsagaraki, M Nafouti, H. Peyre, K Vamvoukakis, **N Makris**, et al.. "Cross-section doping topography of 4H-SiC VJFETs by various techniques", International Conference on Silicon Carbide and Related Materials (ICSCRM 2017), Sep 2017, Washington, DC, United States.
6. **(Best Paper Award)** A. Nikolaou, M.Bucher, **N. Makris**, A. Papadopoulou, L. Chevas et al., "Modeling of High Total Ionizing Dose (TID) Effects for Enclosed Layout Transistors in 65 nm Bulk CMOS," 2018 International Semiconductor Conference (CAS), Sinaia, 2018, pp. 133-136. doi: 10.1109/SMICND.2018.8539806